In the Claims

Please amend the claims as follows:

1. (Currently Amended) A method of data transfer between a source port and a destination port of a transfer controller with plural ports, said method comprising the steps of:

in response to a data transfer request, querying said destination port to determine if said destination port is capable of receiving data of a predetermined size;

if said destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said data transfer request and not transferring data to said destination port until said destination port is capable of receiving data, and

if said destination port is capable of receiving data of said predetermined size, reading data of said predetermined size from said source port and transferring said read data to said destination port.

2. (Currently Amended) The method of claim 1, wherein each port includes at least one write reservation station, said method wherein:

said step of querying said destination port includes:

determining whether any write reservation station of said destination port has not been allocated for receipt of data, ~~and~~

if at least one write reservation is not allocated for receipt of data, determining said destination port can receive data and allocating a write reservation station for receipt of data; and

said step of transferring said read data to said destination port includes transferring said read data to said allocated write reservation station of said destination port.

3. (Original) The method of claim 2, further comprising:

transferring data from a write reservation station storing data to be transferred to an application unit coupled to said destination port at a data transfer rate of said application unit; and

disallocating said write reservation station upon transfer of data to said application unit.

4. (Original) The method of claim 2, wherein:

said step of allocating a write reservation station includes storing a data identifier corresponding to said write reservation station; and

said step of transferring said read data to said destination port includes storing said read data in a write reservation station having a data identifier corresponding to said read data.

5. (Currently Amended) The method of claim 1, further comprising:

while waiting until said destination port is capable of receiving data

determining if a second data transfer request is pending between said source port and a second destination port, and

if a second data transfer request is pending~~, servicing said second data transfer~~

querying said second destination port to determine if said second destination port is capable of receiving data of said predetermined size,

if said second destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said second data transfer request until said second destination port is capable of receiving data, and

if said second destination port is capable of receiving data of said predetermined size, reading data of said predetermined size from said source port and transferring said read data to said second destination port.

6. (Canceled)

7. (Currently Amended) A data transfer controller comprising:

a request queue controller receiving, prioritizing and dispatching data transfer requests, each data transfer request specifying a data source, a data destination and a data quantity to be transferred;

a data transfer hub connected to request queue controller effecting dispatched data transfer requests;

a plurality of ports, each of said plurality of ports having an interior interface connected to said data transfer hub and an exterior interface configured for an external memory/device expected to be connected to said port, said interior interface and said exterior interface operatively connected for data transfer therebetween; and

said data transfer hub controlling data transfer from a source port corresponding to said data source to a destination port corresponding to said data destination in a quantity corresponding to said data quantity to be transferred of a currently executing

data transfer request, said data transfer hub further controlling said source port and said destination port to

in response to a data transfer request, query said destination port to determine if said destination port is capable of receiving data of a predetermined size~~,~~,

if said destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said data transfer request and not transferring data to said destination port until said destination port is capable of receiving data, and

if said destination port is capable of receiving data of said predetermined size, reading data of said predetermined size from said source port and transferring said read data to said destination port.

8. (Currently Amended) The data transfer controller of claim 7, wherein:

each port includes at least one write reservation station for storing data prior to transfer to said corresponding external memory/device;

said data transfer hub further controlling said destination port to

determine whether any write reservation station of said destination port has not been allocated for receipt of data, ~~and~~

if at least one write reservation is not allocated for receipt of data, determining said destination port can receive data and allocating a write reservation station for receipt of data, and

transfer said read data to said allocated write reservation station of said destination port.

9. (Original) The data transfer controller of claim 8, wherein:

said data transfer hub further controlling said destination port to

transfer data from a write reservation station to said corresponding external memory/device at a data transfer rate of said external memory/device, and

disallocating said write reservation station upon transfer of data from said write reservation station to said external memory/device.

10. (Currently Amended) The data transfer controller of claim 8, wherein:

each of said plurality of ~~hubs~~ ports further includes an identifier register corresponding to each write reservation station; and

said data transfer hub further controlling said destination port to

allocate a write reservation station by writing identifier data in said corresponding identifier register, and

store said read data in a write reservation station having a corresponding identifier stored in said identifier register corresponding to said write reservation station.

11. (Currently Amended) The data transfer controller of claim ~~1~~ 7, wherein:

said data transfer ~~controller~~ hub further capable ~~of servicing a second transfer request between said source port and a second destination port~~ while waiting until said destination port is capable of receiving data of

determining if a second data transfer request between said source port and a second destination port is pending,

if a second data transfer request is pending

querying said second destination port to determine if said second destination port is capable of receiving data of said predetermined size,

if said second destination port is not capable of receiving data, waiting by not reading data of said predetermined size from said source port corresponding to said second data transfer request until said second destination port is capable of receiving data, and

if said second destination port is capable of receiving data, reading data of said predetermined size from said source port and transferring said read data to said second destination port.

12. (Canceled)

13. (Currently Amended) A data processing system comprising:

a plurality of data processors, each data processor capable of generating a data transfer request;

a request queue controller connected to said plurality of data processors, said request queue controller receiving, prioritizing and dispatching data transfer requests, each data transfer request specifying a data source, a data destination and a data quantity to be transferred;

a data transfer hub connected to request queue controller effecting dispatched data transfer requests;

a plurality of ports, each of said plurality of ports having an interior interface connected to said data transfer hub identically configured for each port and an exterior interface configured for an external memory/device expected to be connected

to said port, said interior interface and said exterior interface operatively connected for data transfer therebetween; and

said data transfer hub controlling data transfer from a source port corresponding to said data source to a destination port corresponding to said data destination in a quantity corresponding to said data quantity to be transferred of a currently executing data transfer request, said data transfer hub further controlling said source port and said destination port to

in response to a data transfer request, query said destination port to determine if said destination port is capable of receiving data of a predetermined size~~,~~,

if said destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said data transfer request and not transferring data to said destination port until said destination port is capable of receiving data, and

if said destination port is capable of receiving data of said predetermined size, reading data of said predetermined size from said source port and transferring said read data to said destination port.

14. (Currently Amended) The data processing system of claim 13, wherein:

each port includes at least one write reservation station for storing data prior to transfer to said corresponding external memory/device;

said data transfer hub further controlling said destination port to

determine whether any write reservation station of said destination port has not been allocated for receipt of data, ~~and~~

if at least one write reservation is not allocated for receipt of data, determining said destination port can receive data and allocating a write reservation station for receipt of data, and

transfer said read data to said allocated write reservation station of said destination port.

15. (Original) The data processing system of claim 14, wherein:

said data transfer hub further controlling said destination port to

transfer data from a write reservation station to said corresponding external memory/device at a data transfer rate of said external memory/device, and

disallocate said write reservation station upon transfer of data from said write reservation station to said external memory/device.

16. (Original) The data processing system of claim 14, wherein:

each of said plurality of hubs further includes an identifier register corresponding to each write reservation station; and

said data transfer hub further controlling said destination port to

allocate a write reservation station by writing identifier data in said corresponding identifier register, and

store said read data in a write reservation station having a corresponding identifier stored in said identifier register corresponding to said write reservation station.

17. (Currently Amended) The data processing system of claim 13, wherein:

said data transfer ~~controller~~ hub further capable ~~of servicing a second transfer request between said source port and a second destination port~~ while waiting until said destination port is capable of receiving data of

determining if a second data transfer request between said source port and a second destination port is pending,

if a second data transfer request is pending

querying said second destination port to determine if said second destination port is capable of receiving data of said predetermined size,

if said second destination port is not capable of receiving data, waiting by not reading data of said predetermined size from said source port corresponding to said second data transfer request until said second destination port is capable of receiving data, and

if said second destination port is capable of receiving data, reading data of said predetermined size from said source port and transferring said read data to said second destination port.

18. (Canceled)

19. (Currently Amended) The data processing system of claim 13, further comprising:

said plurality of ports includes an internal port master;

a data transfer bus connected to said internal port master and each of said data processors, said data transfer bus transferring data between said plurality of data processors and said data transfer hub via said internal port master;

a system memory connected to a predetermined one of said plurality of ports; and

wherein each of said data processors includes an instruction cache connected to said data transfer bus for temporarily storing program instructions controlling said data processor, said data processor generating a data transfer request to said request queue controller for ~~program~~ instruction cache fill from said system memory to said instruction cache upon a read access miss to said instruction cache.

20. (Currently Amended) The data processing system of claim 13, further comprising:

said plurality of ports includes an internal port master;

a data transfer bus connected to said internal port master and each of said data processors, said data transfer bus transferring data between said plurality of data processors and said data transfer hub via said internal port master;

a system memory connected to a predetermined one of said plurality of ports; and

wherein each of said data processors includes a data cache connected to said data transfer bus for temporarily storing data employed by said data processor, said data processor generating a data transfer request to said request queue controller for data cache fill from said system memory to said data cache upon a read access miss to said data cache.

21. (Currently Amended) The data processing system of claim 13, further comprising:

said plurality of ports includes an internal port master;

a data transfer bus connected to said internal port master and each of said data processors, said data transfer bus transferring data between said plurality of data processors and said data transfer hub via said internal port master;

a system memory connected to a predetermined one of said plurality of ports; and

wherein each of said data processors includes a data cache connected to said data transfer bus for temporarily storing data employed by said data processor, said data processor generating a data transfer request to said request queue controller for data writeback from said data cache to said system memory upon a write miss to said data cache.

22. (Currently Amended) The data processing system of claim 13, further comprising:

said plurality of ports includes an internal port master;

a data transfer bus connected to said internal port master and each of said data processors, said data transfer bus transferring data between said plurality of data processors and said data transfer hub via said internal port master;

a system memory connected to a predetermined one of said plurality of ports; and

wherein each of said data processors includes a data cache connected to said data transfer bus for temporarily storing data employed by said data processor, said data processor generating a data transfer request to said request queue controller for write data allocation from said system memory to said data cache upon a write miss to said data cache.

23. (Currently Amended) The data processing system of claim 13, further comprising:

said plurality of ports includes an internal port master;

a data transfer bus connected to said internal port master and each of said data processors, said data transfer bus transferring data between said plurality of data processors and said data transfer hub via said internal port master;

a system memory connected to a predetermined one of said plurality of ports; and

wherein each of said data processors includes a data cache connected to said data transfer bus for temporarily storing data employed by said data processor, said data processor generating a data transfer request to said request queue controller for data writeback from said data cache to said system memory upon eviction of dirty data from said data cache.

24. (Original) The data processing system of claim 13, wherein:

said plurality of data processors, said request queue controller, said data transfer hub and said plurality of ports are disposed on a single integrated circuit.

25. (Currently Amended) The data processing system of claim 13, further comprising:

a data memory having a data transfer bandwidth on the same order as a data transfer bandwidth of said data transfer hub;

~~a second~~ an internal memory port connected to said data transfer hub and said data memory; and

said data transfer hub further controlling said source port and said destination port to not query said ~~second~~ internal memory port to determine if said destination port is capable of receiving data of a predetermined size if said ~~second~~ internal memory port is a destination port of a data transfer request.